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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/044,394	01/11/2002	Kenneth M. Wilson	10012382-1 9298		
7590 03/12/2004			EXAMINER		
HEWLETT-PACKARD COMPANY			HO, THANG H		
Intellectual Property Administration P.O. Box 272400			ART UNIT	PAPER NUMBER	
Fort Collins, CO 80527-2400			2188	2	
			DATE MAILED: 03/12/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

					Pla				
	1	Application No		Applicant(s)					
		10/044,394		WILSON ET AL.					
Office Action Summary		Examiner	·	Art Unit					
		Thang H Ho		2188					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
THE - External after of the control	ORTENED STATUTORY PERIOD FOR REPL' MAILING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. In period for reply specified above is less than thirty (30) days, a reply or period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing led patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, how y within the statutory miwill apply and will expire a cause the application	vever, may a reply be tim inimum of thirty (30) days SIX (6) MONTHS from to to become ABANDONED	ely filed s will be considered timel the mailing date of this c O (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) filed on 11 Ja	anuary 2002.							
2a) <u></u> ☐	☐ This action is FINAL . 2b) ☐ This action is non-final.								
3)□	☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Disposit	ion of Claims								
4)⊠	4)⊠ Claim(s) <u>1-32</u> is/are pending in the application.								
	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)□	Claim(s) is/are allowed.								
6)⊠	☑ Claim(s) <u>1-32</u> is/are rejected.								
7)🖂	☑ Claim(s) <u>1</u> is/are objected to.								
8)[Claim(s) are subject to restriction and/o	r election require	ement.						
Applicat	ion Papers								
9) The specification is objected to by the Examiner.									
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.									
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority (under 35 U.S.C. § 119								
121	Acknowledgment is made of a claim for foreign	priority under 3!	5 U.S.C. & 119(a)	-(d) or (f)					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:									
1. Certified copies of the priority documents have been received.									
	2. Certified copies of the priority document			on No					
	3. Copies of the certified copies of the prior		* *	-	Stage				
	application from the International Bureau	•			2.2.9.2				
* See the attached detailed Office action for a list of the certified copies not received.									
Attachme	st(e)								
Attachmer 1) Notice	n(s) ce of References Cited (PTO-892)	41	Interview Summary	(PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date									
	3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) 6) Other:								
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Art Unit: 2188

DETAILED ACTION

Information Disclosure Statement

1. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Specification

- 2. Claims 1-32 are presented for examination.
- 3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is required in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

The recitation of "determining the access time should be changed to read -- determining an access time--.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

Art Unit: 2188

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 10/044364 (hereinafter 364). Although the conflicting claims are not identical, they are not patentably distinct from each other because both memory systems comprise substantially the same elements of a system and method for managing a memory system having a plurality of subsystems comprising means for determining an access time to acquire the data from the memory system, comparing the access time to a threshold; and taking actions based on the results of the comparison. One of ordinary skill in the art can readily see that the limitations of the instant application are the same with slight obvious modifications to claim language of limitations of 364. For example, the limitation of claim 1 of the instant application and claims 1 and 13 of the 364 application are the same with slight obvious modifications to claim language.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Page 3

Art Unit: 2188

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 7. Claims 1-2, 13-14 and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (United States Patent 5,784,582).

Hughes discloses a system and method for managing access latency by prioritizing memory access requests among a plurality of data paths based on configuration parameters, wherein the configuration parameters comprise location, size and direction of the transfer in combination with information of the current request.

As per claims 1 and 23, Hughes discloses a system and method substantially as claimed comprising the steps of: upon accessing the memory system for a piece of data used by a first process [i.e., request] determining an access time to acquire the piece of data in the memory system; comparing [i.e., selecting] the determined access time to a threshold [i.e., based on the parameter provided to the selection processor 108 by the control state registers 109 (Figure 3; column 5, lines 46-48)]; and taking actions based on the results of the comparing step; wherein accessing the subsystems is in an non-sequential order [i.e., selecting request according to the parameters including location,

Art Unit: 2188

size and direction of the transfer of the current access (Figure 4; column 2, lines 10-43; column 5, line 63 through column 6, line 5; and column 6, lines 46-49)].

As per claim 2 and 24, Hughes discloses that the data blocks containing the piece of data is placed in the memory system based on information selected in one or a combination of: a movement pattern of data in a data block, a structure of the memory system, and a cache-level architecture in the memory system [i.e., selecting request according to the parameters including location, size and direction of the transfer of the current access (Figure 4, column5, line 63 through column 6, line 5; and column 6, lines 46-49)]

As per claims 13-14, the claims are directed to a computer readable medium carrying instructions, which perform the steps of implementing the process of claims 1-2. Hard drives and memories are computer readable mediums in addition to CD-ROMs, floppy disks, etc. Hughes teaches a computer implemented process, thus it is inherent that the program accomplishing the procedures must be carried or stored on a computer readable medium to enable the computer to function in the manner taught by Hughes.

8. Claims 1-2, 13-14 and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Lamberts (United States Patent 6,418,510).

Lamberts discloses a system and method for memory management that makes cache decisions based on a cost function wherein the cost function is calculated as a

Art Unit: 2188

function of cache access time. Data with higher cost (i.e., higher access time) is added to or kept in the cache while data with lower cost (i.e., lower access time) is not stored in the cache.

As per claims 1 and 23, Lamberts discloses the method substantially as claimed comprising the steps of: upon accessing the subsystems for a piece of data used by a first process, determining the access time to acquire the piece of data in the memory system [i.e., Calculate cost, (Figure 3, references 58 and 60; Figure 4, references 90 and 92)]; comparing the determined access time to a threshold [i.e., Does data block have lowest cost function (Figure 3, element 62 and 66; Figure 4, reference 94 and 98)]; and taking an action based on the results of the comparing step [i.e., whether to cache new data block]; wherein accessing the subsystems is in a non-sequential order [(Figure 3, references 64, 68, 70 and 72; Figure 4, references 96, 100, 102 and 104); column 4, lines 29-55].

As per claim 2 and 24, Lamberts discloses that the data blocks containing the piece of data is placed in the memory system based on information selected in one or a combination of: a movement pattern of data in a data block, a structure of the memory system, and a cache-level architecture in the memory system [see Figure 5 and column 9, line 24 through column 10, line 28]

As per claims 13-14, the claims are directed to a computer readable medium carrying instructions, which perform the steps of implementing the process of claims 1-2. Hard drives and memories are computer readable mediums in addition to CD-ROMs,

Art Unit: 2188

floppy disks, etc. Lamberts teaches a computer implemented process, thus it is inherent that the program accomplishing the procedures must be carried or stored on a computer readable medium to enable the computer to function in the manner taught by Lamberts.

Claim Rejections - 35 USC § 103

- 9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 10. Claims 3-5, 15-17 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (United States Patent 5,784,582) and Frank et al. (United States Patent 5,297,265), hereinafter Frank.

As per claims 3-5 and 25-27, Hughes teaches the method for managing a memory system substantially as claimed. However, Hughes does not specifically teach using a memory table having entries to convert a location address corresponding to an entry pointing to the location of the piece of access data, wherein the memory table working with a memory manager managing the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system. Frank teaches a system and method for using a memory table [i.e. cache directory] to convert a location address corresponding to an entry pointing to the location of the piece of access data [see Figure 5 and column 11, line 23 through column 12, line 68]. Accordingly, it would have been obvious for one skilled in the art at the



Art Unit: 2188

time the invention was made to implement the system and method for managing a memory system as taught by Hughes and to utilize a memory table as taught by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37.

As per claims 15-17, the claims are directed to a computer readable medium carrying instructions, which perform the steps of implementing the process of claims 3-5. Hard drives and memories are computer readable mediums in addition to CD-ROMs, floppy disks, etc. Hughes teaches a computer implemented process, thus it is inherent that the program accomplishing the procedures must be carried or stored on a computer readable medium to enable the computer to function in the manner taught by Hughes.

11. Claims 6-8, 11, 18-19, 21, 28-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamberts (United States Patent 6,418,510) and Eickemeyer et al. (United States Patent 6,049,867), hereinafter Eickemeyer.

As per claims 6-8, 11, 28-29 and 31 Lamberts teaches the method for managing a memory system substantially as claimed including the steps of comparing the time taken to complete the memory access to a threshold [i.e. determining whether to overwrite data based on the estimated access time (see Figure 3 and Figure 4)]; and if the time taken to complete the memory access is close to, equal to, or greater than the threshold, then taking an action [i.e., whether to cache new data block] [(Figure 3,

Art Unit: 2188

references 64, 68, 70 and 72; Figure 4, references 96, 100, 102 and 104); column 4, lines 29-55]. However, Lamberts does not specifically teach the method of accessing the memory system for a piece of data used by a first process, a processor working with the memory system continuing its functions until it is stalled. Eickemeyer teaches a system and method for memory management to reducing memory access latency utilizing a process or thread switch to allow the switching between multiple threads in response to the occurrence of an event such as a cache miss or stall that indicates long memory latency may occur. In an event of a cache miss, a first thread is suspended allowing a second thread to access the cache memory [Abstract, column 4, lines 27-55; and column 5, lines 4-7]. Accordingly, it would have been obvious for one skilled in the art at the time the invention was made to implement the system and method for managing a memory system as taught by Lamberts and incorporate Eickemeyer's teachings to include a process switch to postpone of a current process and allow a second process to execute in an event of a cache miss. One skilled in the art would have been motivated to do so, because the utilization of a process switch provides further memory access latency reduction and eliminates the need for complex, replication of pipeline latches and pipeline states rendering a cost-effective system as pointed out by Eickemyer on column 4, line 27 through 55.

As per claims 18-19, and 21, the claims are directed to a computer readable medium carrying instructions, which perform the steps of implementing the process of claims 6-8. Hard drives and memories are computer readable mediums in addition to

Art Unit: 2188

CD-ROMs, floppy disks, etc. Lamberts teaches a computer implemented process, thus it is inherent that the program accomplishing the procedures must be carried or stored on a computer readable medium to enable the computer to function in the manner taught by Lamberts.

12. Claims 9-10, 12, 20, 22, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamberts (United States Patent 6,418,510) and Eickemeyer et al. (United States Patent 6,049,867), hereinafter Eickemeyer as applied to claims 6, 11, 18, 21, 28 and 31 above, respectively, and further in view of Frank et al. (United States Patent 5,297,265), hereinafter Frank.

As per claims 9-10, 12, 30 and 32, Lamberts and Eickemeyer teaches the system and method as recited as detailed above. However, neither Lamberts nor Eickemeyer teaches the usage of a memory table having entries to convert a location address corresponding to an entry pointing to the location of the piece of access data, wherein the memory table working with a memory manager managing the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system. Frank teaches a system and method for using a memory table [i.e. cache directory] to convert a location address corresponding to an entry pointing to the location of the piece of access data [see Figure 5 and column 11, line 23 through column 12, line 68]. Accordingly, it would have been obvious for one skilled in the art at the time the invention was made to implement the system and method for managing a memory system as taught by Hughes and to utilize a memory table as taught

Art Unit: 2188

by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37.

As per claims 20 and 22, the claims are directed to a computer readable medium carrying instructions, which perform the steps of implementing the process of claims 9-10. Hard drives and memories are computer readable mediums in addition to CD-ROMs, floppy disks, etc. Lamberts teaches a computer implemented process, thus it is inherent that the program accomplishing the procedures must be carried or stored on a computer readable medium to enable the computer to function in the manner taught by Lamberts.

Conclusion

- 13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.
- 14. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Art Unit: 2188

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho Art Unit 2188 March 5, 2004 Man Lambanashan Mano PADMANASHAN SUBBEUBORY PATENT EDAMINDE TERIOR